**Collar Board Schematic and Layout Notes**

Main Board:

* 1.1V Converter
* BUCK Converter With Boost
* 50MHz CLOCK
* CPLD
* FLASH
* FPGA
* External Serial Plug
* Octal Buffers
* SDRAM

Sensor Board:

* Inertial Module
  + 5 data lines at 1.8V
  + 2 control lines
* GPS
  + 4 data lines at 3.3V
  + 1 control line
* Microphones
  + 3 data lines at 3.3V
  + 2 control lines
* SD Card
  + 6 data lines at 3.3V
  + 1 control line without level shifter
* Data Transfer
  + 5 data lines at 3.3V
  + 1 control line
* Solar Controller
  + 2 control lines
  + 1 buffered control line
* Battery Monitor
  + 3 control lines
  + I2C
* MRAM
  + 5 data lines at 3.3V
  + 1 control line
* Real Time Clock
  + 1 control line
  + I2C
* Power Switches
  + 2 buffered control lines

Total 1.8V I/O Pins: 14 used of the 16 available

Total 3.3V I/O Pins: 20 used of the 21 available

Total control lines: 14 used of the 16 available + I2C

Total buffered control lines: 3 used of the 3 available

**Bank Voltages (FPGA):**

The bank voltages were chosen based on best fit for the physical layout and requirements for the SENSOR board.

**2A:** 1.8V

**3A:** 1.8V

**3B:** 3.3V

-I/O Lines: M\_FPGA\_3B\_[0-13]

**4A:** 3.3V

-I/O Lines: M\_FPGA\_4A\_[0-9]

**5A:** 1.8V

**5B:** 1.8V

**7A:** 1.8V

- I/O Lines: M\_FPGA\_7A\_[0-12]

**8A:** 1.8V

-I/O Lines: M\_FPGA\_8A\_[0]

**Control Lines (CPLD lines):**

M\_CPLD\_[0-15]

CPLDON\_[0-2] (Buffered lines)

**MAIN Board Notes**

*1/2/15:*

* *Replaced feedback resistors with 0402 equivalents*

*1/9/15:*

* *Replaced all but 1.1V feedback resistors and FPGA capacitors with 0402 equivalents.*
* *Made CPLD decoupling caps 0201’s.*
* *Updated components to have Digi-Key ordering number.*

*1/10/15 – 2/8/15:*

* *Completely forget about this document.*
* *Swapped all but the FPGA capacitors for unique components with DigiKey ordering parts for easier generation of BoM*
* *Removed isolated power plane for VCCPGM*

*2/9/15:*

* *Added the Transceiver circuity to the schematic.*
* *Circuitry connections based on CC112xEM\_868\_915 evaluation board.*

*2/12/15:*

* *I2C header designed to be 4 pads, CLK, DATA, GND,VCC.*
  + *VCC and GND will be pins 1 and 4 with CLK and DATA in-between the two to prevent accidental grounding of power*
  + *Pads have been chosen over through holes as they allow for routing below them and component placement on the other side of the board. The pads have arbitrary sizes of 80x80mils with 100mils in between.*
* *The isolated 2.5V power plane for the PLL will stay on the board*

*2/13/15:*

* *The SENSOR board will have 10 additional holes to accommodate wires to a potential external connector. These holes will have the same connections as the 10 pin connector on the MAIN board*
* *Battery will just be 2 holes. Wires will be soldered to these holes and the battery will be connected off-board*
* *Solar cell connection will just be 2 holes. Similar design as battery*
* *General signal naming for the schematic*
  + *M\_FPGA\_[Bank]\_[Bank Pin #] ex. M\_FPGA\_5B\_7*
  + *M\_CPLD\_[I/O #] ex. M\_CPLD\_7*
* *Power and GND pins going in between the two boards 18 total*
  + *1 pin per connector per power plane*
    - *4 pins for 3.3V*
      * *2 pins for VCC 3.3V*
      * *2 pins for FPGA\_VCC3.3V*
    - *4 pins for 2.5V*
      * *2 pins for VCC2.5V*
      * *2 pins for FPGA\_VCC2.5V*
    - *4 pins for 1.8V*
      * *2 pins for VCC1.8V*
      * *2 pins for FPGA\_VCC1.8V*
    - *2 pins for 1.1V*
      * *2 pins for VCC 1.1V*
  + *4 GND Pins*
* 2x50pin connectors (PN: 52991-0508)
  + Clearance of 4mm
    - This clearance is chosen because the USB 3.0 header is 2.5mm and will be inbetween the two boards to minimize skyline
  + 50 pins chosen because it fit on the board and it was the only connector of sufficient number of pins that was in stock as of today

2/19/15:

* One of the FPGA banks will have its VCCIO pins connected to 1 pin on the board connector as well as being connected to a jumper. The VCCPD will be connected to 1 pin on the board connector and connected to a jumper
  + If the jumper is not set the pins will go to 50 pin header so that its voltage may be determined from a daughter board.
  + If the jumper is set it will short the pins to 3.3V
* There is a jumper on the AUX\_VCC pin of the 10pin header.
  + If the jumper is selected it will short the incoming 5V USB to the PWR\_MAIN (Previously called BATTERY\_PACK\_PLUS) BUS.
  + If the jumper is not shorted then it will output to 4 PWR\_AUX pins on the header
  + 4 PWR\_MAIN pins will take in power from the header

2/22/15:

* All signals and power (with the exception of GND) coming from the External Serial Header will have prefix ESH\_ to denote that they are connected directly to the External Serial Header

2/23/15:

* Connected CLK\_50MHZ\_TO\_FPGA to a CLK[0:11]p pin as well as a regular I/O pin as specified in the *Cyclone® V Device Family Pin Connection Guidelines* for use with the PLL.
* Potentially add O-buff enable to header
* Add buffered lines to header

3/14/15:

* Duplicate data lines from flash to cpld

3/17/15:

* Added 2 more 10k Resistors to each board. More will need to be ordered
* Added VCC1P8\_AUX for I2C pull-ups. The voltage is a separate 1.8V power that is separate from the FPGA power and the regular power. Currently being used for I2C but may be used for other unknown devices
  + This will require an addition 4.7uF and 0.1uF cap
* Added an addition 2 pin to AUX\_POWER for a total of 4 pins
* Added an additional 2 pins to PWR\_MAIN for a total of 4 pins
* Added the pins from the 10 pin header to the board connectors taking an additional 8pins

Routing for this board was then completed please see MCollar\_MAIN\_v1Specs.doc for the final design details

**SENSOR Board Notes**

5/26/15:

* For small low pins count BGA packages Via in Pad is best to use to break out inner pins as opposed to 3mil trace/space.
  + “Better control of the process. With .003” traces and spacing, when considering we need to increase the size/width of your design in order to account for the etch process, there is higher probability of scrap due to over or under etching that causes either opens and/or shorts.”
* Due to lack of feedback from Andy I will proceed with designing the Data TRX board according to the *SWRC222* recommended layout and design from the *CC1120* data sheet.

5/27/15:

* The GPS antenna needs to be placed “Sideways” at the side of the board facing up
  + Parts under the GPS antennae need to be considered, it is possible that the SENSOR board may be extended so that the GPS antenna overhangs the MAIN board as opposed to sitting right on top of it
* The Data TRX antenna interface will also be place on the side of the board facing up
  + Current antenna interface is just a single through hole that can accommodate 20 Gauge wire
* The Top of the board is determined to be the side with the GPS and data TRX antenna
* The GPS is placed on the bottom layer of the SENSOR board on the opposite side of the External Serial Header plug of the MAIN board.
  + The GPS has a clearance of 2.7mm and the uUSB plug has a clearance of 2.8mm. The total clearance between the boards is 4mm.
  + GPS placed on the bottom layer to reduce vertical skyline
* uSD card holder placed on the top layer of the SENSOR board on the same side as the uUSB plug
  + This is done because it will allow for a single interface port on the collar to access both the plug and the SD card
* All other parts are currently best fit given the above restrictions
* Confirmed with Andy that the first revision of the Data TRX test board will follow the *SWRC222* recommended layout and design from the *CC1120* data sheet.
  + This board will have the Data TRX placed in approximately the same location that it is on the SENSOR board
  + The board will have 100mil header holes to access data lines as well as power and ground pins
    - Power will connect to the power plane *after* the power switch so using the power switch will not be nessesarry to use the board if the user does not want to use the MAIN board interface at the time
  + The board will have a power switch to control the component
  + It will also be hooked up so it can interface with the MAIN board if desired.

5/28/15:

* Checked cost calculations for ViP process because it is a required process for our board
  + Using extra ViP does not add incremental cost as long as the board does not become excessive with the vias that require the ViP process.
    - This means it is recommended to potentially use ViP for the 50pin board connectors

6/2/15:

* The SENSOR board was extended about a quarter inch to accommodate the GPS and data TRX antenna. This will allow the antenna to overhang the MAIN board and potentially provide better reception.

6/3/15:

* The microphones will not be placed on the SENSOR board
  + Instead there will be 4 pads for each mic (PWR,GND, CLK, and, DATA) that will interface with the microphones off board.
* The microphones will be on their own set of separate boards.
* There will be a PCB that accommodates the battery and potentially the Serial Header lines to interface with this we will have a 17 pad header
  + 2 pins for ESH\_AUX\_VCC
  + 1 pin for ESH\_FPGA\_USB\_DMINUS
  + 1 pin for ESH\_FPGA\_USB\_DPLUS
  + 1 pin for ESH\_FORCE\_STARTUP
  + 2 pins for GND
  + 1 pin for ESH\_FPGA\_SPI\_CLK
  + 1 pin for ESH\_JTAG\_TCK
  + 1 pin for ESH\_JTAG\_TMS\_SPI\_CS
  + 1 pin for ESH\_JTAG\_TDI\_SPI\_MOSI
  + 1 pin for ESH\_JTAG\_TDO\_SPI\_MISO
  + 1 pin for THERMISTOR\_PLUS
  + 2 pins for BATTERY\_PLUS
  + 2 pins for BATTERY\_MINUS
  + We will be using 28 gauge wire which can handle about .25 Amps continuous. So to handle the power consumption required to run our system our power and ground lines will require 2 wires

6/9/15:

* Added a 10uF capacitor the power pin of the SDCard to accommodate for initial power draw of the device when it starts up.
* Added both a 4bit MUX and 4bit Level shifter to the Data TRX circuitry
  + This circuitry will be used to allow for switching between the FPGA and the CPLD talking to the data transmitter
    - When the FPGA is on the MUX will allow the FPGA to talk to the data transmitter
    - When the FPGA is off the MUX will allow the CPLD to talk to the data transmitter
    - The level shifter will boost the 1.8V signal coming out of the CPLD to the necessary 3.3V signals needed to communicate with the data TRX

6/10/15:

* The “\_TO\_FPGA” suffix on a signal name in the schematic indicates that a signal is going to the FPGA logic. Same with the “\_TO\_CPLD” suffix

6/11/15:

* Added 0.1uF power capacitors to the power lines of the GPS
  + 0.1uF is standard decoupling size and recommended by the data sheet and application development kit.
* Added 1uF power capacitor to the power line of the MRAM
  + 1uF is chosen because MRAM has power spikes of up to 25mA at 1Mhz as specced by the data sheet