**Collar Board Schematic and Layout Notes**

Main Board:

* 1.1V Converter
* BUCK Converter With Boost
* CLOCK
* CPLD
* FLASH
* FPGA
* uUSB 3.0
* Octal Buffer
* SDRAM

Sensor Board:

* Inertial Module 12 Lines
* GPS 5 Lines
* Microphones 3 Lines (May not be on board)
* SD Card 8 Lines
* Data Transfer 6 Lines
* Solar Controller 2 Lines (Update Schematic appropriately)
* Battery Monitor ~5 Lines (Update Schematic appropriately)
* MRAM 6 Lines
* Real Time Clock 3 Lines

*1/2/15:*

* *Replaced feedback resistors with 0402 equivalents*

*1/9/15:*

* *Replaced all but 1.1V feedback resistors and FPGA capacitors with 0402 equivalents.*
* *Made CPLD decoupling caps 0201’s.*
* *Updated components to have Digi-Key ordering number.*

*1/10/15 – 2/8/15:*

* *Completely forget about this document.*
* *Swapped all but the FPGA capacitors for unique components with DigiKey ordering parts for easier generation of BoM*
* *Removed isolated power plane for VCCPGM*

*2/9/15:*

* *Added the Transceiver circuity to the schematic.*
* *Circuitry connections based on CC112xEM\_868\_915 evaluation board.*

*2/12/15:*

* *I2C header designed to be 4 pads, CLK, DATA, GND,VCC.*
  + *VCC and GND will be pins 1 and 4 with CLK and DATA in-between the two to prevent accidental grounding of power*
  + *Pads have been chosen over through holes as they allow for routing below them and component placement on the other side of the board. The pads have arbitrary sizes of 80x80mils with 100mils in between.*
* *The isolated 2.5V power plane for the PLL will stay on the board*

*2/13/15:*

* *The SENSOR board will have 10 additional holes to accommodate wires to a potential external connector. These holes will have the same connections as the 10 pin connector on the MAIN board*
* *Battery will just be 2 holes. Wires will be soldered to these holes and the battery will be connected off-board*
* *Solar cell connection will just be 2 holes. Similar design as battery*
* *General signal naming for the schematic*
  + *M\_FPGA\_[Bank]\_[Bank Pin #] ex. M\_FPGA\_5B\_7*
  + *M\_CPLD\_[I/O #] ex. M\_CPLD\_7*
* *Power and GND pins going in between the two boards 18 total*
  + *1 pin per connector per power plane*
    - *4 pins for 3.3V*
      * *2 pins for VCC 3.3V*
      * *2 pins for FPGA\_VCC3.3V*
    - *4 pins for 2.5V*
      * *2 pins for VCC2.5V*
      * *2 pins for FPGA\_VCC2.5V*
    - *4 pins for 1.8V*
      * *2 pins for VCC1.8V*
      * *2 pins for FPGA\_VCC1.8V*
    - *2 pins for 1.1V*
      * *2 pins for VCC 1.1V*
  + *4 GND Pins*
* 2x50pin connectors (PN: 52991-0508)
  + Clearance of 4mm
    - This clearance is chosen because the USB 3.0 header is 2.5mm and will be inbetween the two boards to minimize skyline
  + 50 pins chosen because it fit on the board and it was the only connector of sufficient number of pins that was in stock as of today

2/19/15:

* One of the FPGA banks will have its VCCIO pins connected to 1 pin on the board connector as well as being connected to a jumper. The VCCPD will be connected to 1 pin on the board connector and connected to a jumper
  + If the jumper is not set the pins will go to 50 pin header so that its voltage may be determined from a daughter board.
  + If the jumper is set it will short the pins to 3.3V
* There is a jumper on the AUX\_VCC pin of the 10pin header.
  + If the jumper is selected it will short the incoming 5V USB to the PWR\_MAIN (Previously called BATTERY\_PACK\_PLUS) BUS.
  + If the jumper is not shorted then it will output to 4 PWR\_AUX pins on the header
  + 4 PWR\_MAIN pins will take in power from the header

2/22/15:

* All signals and power (with the exception of GND) coming from the External Serial Header will have prefix ESH\_ to denote that they are connected directly to the External Serial Header

2/23/15:

* Connected CLK\_50MHZ\_TO\_FPGA to a CLK[0:11]p pin as well as a regular I/O pin as specified in the *Cyclone® V Device Family Pin Connection Guidelines* for use with the PLL.
* Potentially add O-buff enable to header
* Add buffered lines to header